What is claimed is:

1. A flip chip package comprising:

a substrate having an upper surface and a lower surface, the substrate comprising:

a recessed cavity defined in the upper surface of the substrate;

a reinforcement-containing insulating layer;

a plurality of chip contact pads formed on the surface of the reinforcement-containing insulating layer and exposed from the recessed cavity; and

a plurality of solder pads formed on the upper surface of the substrate and outside the recessed cavity for making external electrical connections,

wherein the chip contact pads are electrically connected to the solder pads; and

a semiconductor chip disposed in the recessed cavity of the substrate by flip chip bonding and electrically connected to the chip contact pads.

2. The flip chip package as claimed in claim 1, wherein the semiconductor chip is mechanically and electrically interconnected to the chip contact pads of the substrate via solder joints.

3. The flip chip package as claimed in claim 2, further comprising an underfill formed between the semiconductor chip and substrate.

4. The flip chip package as claimed in claim 1, further comprising a metal coating formed on the lower surface of the substrate and a plurality of conductive vias formed through the reinforcement-containing insulating layer.

5. The flip chip package as claimed in claim 1, further comprising a heat sink disposed on the backside surface of the semiconductor chip.

6. The flip chip package as claimed in claim 1, wherein the reinforcement-containing insulating layer is formed from BT (bismaleimide-triazine) resin.

7. The flip chip package as claimed in claim 1, wherein the reinforcement-containing insulating layer is formed from FR-4 fiberglass reinforced epoxy resin.